A METHOD OF PROVIDING VIA IN A MULTILAYER SEMICONDUCTOR DEVICE

FIELD OF INVENTION

[0001] The present invention relates to a providing via in a multilayer semiconductor device. In several embodiments, the present invention's method of providing via in a multilayer semiconductor device may act to reduce die sawing chipping.

BACKGROUND OF THE INVENTION

[0002] Semiconductor devices are typically fabricated on large semiconductor wafers in multiple passes. Over a fabrication time period, the semiconductor device (also referred to as a die) will be fabricated with multiple layers. Once the fabrication process is complete, the individual circuits must be separated from each other. A typical process for this separation is called scribing.

[0003] Referring now to **Fig. 1**, as will be familiar to those of ordinary skill in the semiconductor fabrication arts, a danger in the separation process is that cracks and other imperfections can develop during the separation process, often as a result of scribing. Pads 10, which are connection points to provide electrical connectivity with the die 2, are often a point where such failures manifest.

[0004] As a partial solution, scribe streets 1 are used which separate adjacent die 2 and are typically arranged in a uniform pattern over the entire wafer. Horizontal and vertical scribe streets 1 are not always identical in width. Scribe streets 1 may vary from around 3 mils to around 7 mils, depending on the process used.

[0005] Pads 10 are typically located on an outside edge of a die 2 and will be located adjacent to the scribe street 1. Many current pad designs of test keys on scribe lines for copper/low-resistence (Cu/low-K) designs enlarge a chipping area when sawing the die on the

wafer. Chipping often occurs along a die edge, resulting in poor reliability or even complete damage to the circuitry on the die.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006] **Fig. 1** is an exemplary schematic view of a die and scribe streets;

[0007] **Fig. 2a** and **Fig. 2b** are schematic illustrations of square and octagonal pad designs of the prior art;

[0008] **Figs. 3a** is a top planar view, and **3b** is a partial view in cross-section of a first embodiment of a pad design of present invention;

[0009] **Figs. 4a** is a top planar view, and **4b** is a partial view in cross-section of a second embodiment of a pad design of present invention;

[0010] **Figs. 5a** is a top planar view, and **5b** is a partial view in cross-section of a third embodiment of a pad design of present invention; and

[0011] **Figs. 6a** is a top planar view, and **6b** is a partial view in cross-section of a fourth embodiment of a pad design of present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0012] In embodiments of the present invention, pad 10 (**e.g., Fig. 1**) comprises a border and inner via design. These embodiments may aid in reducing stress and eliminating crack penetration into a die (e.g., die 2 in **Fig. 1**).

[0013] Referring now to **Fig. 3a** and **Fig. 3b**, in a first embodiment, via 16 for multilayer semiconductor device 2 (**Fig. 1**) are created by providing a first via set on a first layer of semiconductor device 2, e.g. on substrate S. A substantially rectilinear first peripheral border 11,12,13,14 is provided, e.g. fabricated, on first layer S of semiconductor device 2. The interior of first peripheral border 11,12,13,14 defines inner area 15. In a currently envisioned process,

the substantially rectilinear first peripheral border 11,12,13,14 defines a rectangle, a square, an octagon, or the like. Further, in a currently preferred embodiment maximum distance in a single plane of two opposing sides of the substantially rectilinear first peripheral border, e.g. distance D in **Fig. 3a** between border 11 and border 13, is approximately 70 μm.

[0014] A plurality of first via 16 are provided on first layer S within inner area 15 as part of the first via set. As illustrated in **Fig. 3a**, the plurality of first via 16 may be arranged in substantially parallel lines having predetermined width W and predetermined separation distance SD between some or each of first via 16 to adjacent first via 16.

[0015] As a next layer is fabricated for semiconductor device 2 (**Fig. 1**), a subsequent via set, e.g. a second via set, is provided on the next layer of semiconductor device 2. It will be understood that subsequent layers will be disposed above a prior layer, e.g. that, as used herein for exemplary purposes, the second layer will be disposed above the first layer. The second via set may be substantially identical to the first via set and will be disposed substantially parallel to the first via set in a plane defined by the second layer, e.g. the second via set will comprise via 16 that are disposed substantially parallel to and substantially above first via 16 of the first via set. As the second via set is provided, conductive pathway 19 between each of the first via 16 of the first via set and each of the corresponding first via 16 of the second via set is further provided.

[0016] As illustrated in **Fig. 3b**, this process may be continued for each subsequent layer of semiconductor device 2 (**Fig. 1**), resulting in layers of mirrored via 16. As will be understood by those of ordinary skill in the semiconductor fabrication arts, a final layer may be provided which adds conductive pad 18, e.g. a metal or other conductive area to an accessible layer of semiconductor device 2.

[0017] In a first embodiment, substantially rectilinear first peripheral border 11,12,13,14 defines a rectangle, e.g. a square. The plurality of first via 16 comprise slots 17 between via 16 at predetermined separation distances SD. Slots 17 may aid in reducing pad stiffness. First via 16 need not be of uniform widths. In an exemplary embodiment, each side 11,12,13,14 is approximately 5 μm wide. In this embodiment, predetermined width W is approximately 1.5 μm; predetermined separation distance SD between adjacent first via 16 is approximately 1.0 μm; and outermost via 16, e.g. via 16a and via 16b, are separated from their adjacent border, 11 and 13, by approximately 1 μm.

[0018] Referring now to **Fig. 4a** and **Fig. 4b**, in an alternative embodiment, substantially rectilinear first peripheral border 21,22,23,24 defines an rectangle, e.g. a square, where each side 21,22,23,24 is approximately 5 μm wide. However, as opposed to the types and characteristics of the embodiment illustrated in **Fig. 3a** and **Fig. 3b**, two sides, 21 and 23, are substantially uniform. Each of the other two sides 22 and 24 comprises outer edge and inner edge, e.g. outer edge 21a and inner edge 21b, separated by separation distance ESD. Separation distance ESD may acts to release stress.

[0019] In an exemplary embodiment, outer edge 21a and inner edge 21b are each approximately 2 μm wide and ESD is approximately 0.5 μm. Further, in the exemplary embodiment, predetermined width W is approximately 12 μm, leading to wider and fewer first via 26. However, first via 16 need not be of uniform widths. In the exemplary embodiment, separation distance SD between these first via 26 to an adjacent first via 26 is approximately 2.0 μm. Each first via 26 is substantially parallel and adjacent to side 21 and 23. First via 26a and 26b are separated from sides 21 and 23, respectively, by approximately 10 μm.

[0020] Referring now to **Fig. 5a** and **Fig. 5b**, in a further embodiment, a first via set is provided, e.g. fabricated, on a first layer of semiconductor device 2 (**Fig. 1**) by providing first peripheral border 31 on a first layer of semiconductor device 2, e.g. substrate S. The first via set further comprises second peripheral border 33 provided on the first layer where second peripheral border 33 is disposed substantially parallel to first peripheral border 31 at predetermined distance D. First peripheral border 31 and second peripheral border 33 define inner area 35. A plurality of first via 36 are provided on the first layer of semiconductor device 2 within inner area 35 where first via 36 may be arranged in substantially parallel lines having predetermined width W and predetermined separation distance SD to an adjacent first via 36. Further, first via 36 are disposed substantially perpendicular to first peripheral border 31 and second peripheral border 33.

[0021] Subsequent layers of semiconductor device 2 (**Fig. 1**) may possess subsequent via sets, e.g. a second via set will be provided on a second layer of a semiconductor device where the subsequent layer is disposed above the previous layer. For example, the second layer may be disposed on top of the first layer. These subsequent via sets may be provided by providing a via set substantially identical to the prior via set, e.g. the first via set, and disposed substantially parallel to the prior, e.g. first, via set in a plane defined by the second layer. Conductive pathway 39a will be provided between first peripheral border 31 of a prior via set and first peripheral border 31 of subsequent via set. Conductive pathway 39b will likewise be provided between the second peripheral border 33 of the prior via set and second peripheral border 33 of the subsequent via set. Additionally, conductive pathway 39c will be provided between each of first via 36 of the prior via set and each of first via 36 of the subsequent via set which will be disposed substantially parallel to and substantially above first via 36 of the first via set.

[0022] In this embodiment, first peripheral border 31 and second peripheral border 33 may further comprise a repeating inner design, e.g. a substantially sawtooth pattern as illustrated in **Fig. 5a**. Preferably, apex 31b of each tooth 31a of the sawtooth pattern will be conductively connected to a nearest first via 36.

[0023] In currently envisioned embodiments, typical dimensions for first peripheral border 31 and second peripheral border 33 are each approximately 10 μm wide. Inner area 35 is typically approximately 40 μm wide. Predetermined width W is typically approximately 12 μm.

[0024] In one embodiment, the repeating inner design further comprises outer rectilinear portion 31c and an inner pattern of teeth 31a arranged in a substantially sawtooth pattern wherein conductive pathway 39a of first peripheral border 31 is disposed proximate outer rectilinear portion 31c of first peripheral border 31 and conductive pathway 39b of second peripheral border 33 is disposed proximate outer rectilinear portion 33c of second peripheral border 33. In this embodiment, typical values for distance D, from an outer edge of a border 31,33 perpendicularly to a nearest apex, e.g. 31b, is approximately 10 μm and a width of outer rectilinear portion 31c,33c is approximately 4 μm.

[0025] Referring now to **Fig. 6a** and **Fig. 6b**, in a further embodiment, a plurality of bordering elements are provided to aid in blocking a crack in semiconductor device 2 (**Fig. 1**), should one be created during the separation process. In this embodiment, a first via set is provided, e.g. fabricated, on a first layer of semiconductor device 2 by providing first peripheral border 41 and second peripheral border 43 on the first layer of a semiconductor device, where second peripheral border 43 is disposed substantially parallel to first peripheral border 41. Second peripheral border 43 is further disposed at distance D where inner area 45 is defined by the area in between first peripheral border 41 and second peripheral border 43.

[0026] Additional sets of inner borders are provided in inner area 45. First inner border 42a is disposed in inner area 45 substantially parallel to first peripheral border 41 at separation distance D_1 and second inner border 44a disposed in inner area 45 substantially parallel to second peripheral border 43 at separation distance D_1. Further, third inner border 42b is disposed in inner area 45 substantially parallel to first inner border 42a at separation distance D_2 and fourth inner border 44b disposed in inner area 45 substantially parallel to second inner border 42a at separation distance D_2. First via 46 are provided on the first layer of semiconductor device 2 (**Fig. 1**) within inner area 45 in between third inner border 42b and fourth inner border 44b at separation distance D_3 from third inner border 42b and fourth inner border 44b.

[0027] For subsequent layers, subsequent via sets are provided, e.g. a second via set is provided on a second layer of semiconductor device 2 (**Fig. 1**). These subsequent via sets, e.g. the second via set, are disposed on the subsequent layers above the prior layer, e.g. the second via set is disposed above the first via set. For these subsequent via sets, a subsequent via set is provided to be substantially identical to the prior via set with the subsequent via set disposed substantially parallel to the prior via set in a plane defined by the prior layer. Conductive pathway 49a will be provided between first inner border 42a of the prior via set and first inner border 42a of the subsequent via set. Conductive pathway 49b will likewise be provided between third inner border 44a of the prior via set and third inner border 44a of the subsequent via set. Additionally, conductive pathway 49c will be provided between first via 46 of the prior via set and first via 46 of the subsequent second via set.

[0028] In an embodiment, for each via set first peripheral border 41 and second peripheral border 43 are each approximately 5 μm wide; distance D_1 from an outer edge of first peripheral border 41 perpendicularly to a furthest distance on an outer edge of second peripheral

border 43 is approximately 70 μm; first inner border 42a and second inner border 44a are each approximately 2 μm wide; third inner border 42b and fourth inner border 44b are each approximately 2 μm wide; first inner border 42a is separated from each of first peripheral border 41 and third inner border 42b by approximately 2 μm; third inner border 42b is separated from each of second peripheral border 43 and fourth inner border 44b by approximately 2 μm; third inner border 42b and fourth inner border 44b are separated from the inner area by approximately 2 μm; and inner area 45 comprises a rectangle approximately 30 μm wide and 60 μm long.

[0029] In an embodiment, first peripheral border 41 is longer than first inner border 42a, first inner border 42a is longer than third inner border 42b, second peripheral border 43b is longer than second inner border 44a, and second inner border 44a is longer than fourth inner border 44b. In this embodiment, first peripheral border 41 may be substantially the same length as second peripheral border 43, first inner border 42a may be substantially the same length as second inner border 44a, and third inner border 42b may be substantially the same length as fourth inner border 44b.

[0030] In all these embodiments, the order of creation of the via set constituent parts is not critical and the above descriptions should not be read to imply a precise order for creating constituent parts for a via set. Further, the dimensions for the various embodiments given above are for exemplary embodiments and are not limitations of the invention as a whole.

[0031] It will be understood that various changes in the details, materials, and arrangements of the parts which have been described and illustrated above in order to explain the nature of this invention may be made by those skilled in the art without departing from the principle and scope of the invention as recited in the appended claims.